

SPECIFICATION
FOR
EPD MODULE

MODULE NO. : E0470A01-AF-S
Customer NO. :
REVISION : A

AVD	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE			

CUSTOMER APPROVAL	SIGNATURE	DATE

Note:
This specification is subject to change without prior notice in order to improve performance or quality
etc. please contact SHENZHEN` YINGRUIDA CO.,LTD to confirm the latest revision.

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1.General Description

E0470A01-AF-S is an Active Matrix Electrophoretic Display(AM EPD), High-Resolution AM TFT Black/White display module which can be used in portable electronic devices, such as E-book Reader. The module is a TFT-array driving Electrophoretic display, with integrated circuits including source and gate drivers. The resolution of the module is 684×1216, and the active area is 4.7 inch diagonal.

2.Features

- ◆ 684×1216 Resolution
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface

3.Application

E-book reader.

4.Input/Output Pin Assignment

No.	Name	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	NC	NO Connection
5	VDD	Power for digital circuit
6	MODE	Used as gate driver output mode selection pins. MODE = H: Normal single pulse. MODE = L: Always keep VGL.
7	CKV	Clock gate driver
8	SPV	Start pulse gate driver
9	VSS	Ground
10	VCOM	Common Connection
11	VDD	Power for digital circuit
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver

26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Data shift start pulse
32	XLE	Source driver parallel latch enable, transparent when High
33	XOE	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”
34	VDD	Power for digital circuit
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	NC	NO Connection
40	BORDER	VBORDER

5. Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Single ground	VSS		-	0	-	V
Logic Voltage supply	VDD		2.6	3.3	3.6	V
	IVDD	VDD=3.3V	-	1.6	-	mA
Gate Positive supply	VGH		21	22	23	V
	IVGH	VGH=22V	-	0.53	-	mA
Gate Negative supply	VGL		-21	-20	-19	V
	IVGL	VGL=-20V	-	0.56	-	mA
Source Positive supply	VPOS		14.6	15	15.4	V
	IPOS	VPOS=15V	-	0.62	-	mA
Source Negative supply	VNEG		-15.4	-15	-14.6	V
	INEG	VNEG=-15V	-	0.64	-	mA
Asymmetry source	VASYM	VPOS+VNEG	-800	0	800	mV
Common voltage	VCOM		-5	Adjusted	0	V
	ICOM		-	0.14	-	mA
Standby power module	PSTBY		-	-	2	mW
Typical power module	PTYP		-	5.28	-	mW

Notes:

1. The maximum power and maximum current are specified for the worst case power consumption.
2. The typical power is measured when "typical images" are displayed.
3. The standby power is the consumed power when the module controller is in standby mode.
4. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by AVD.

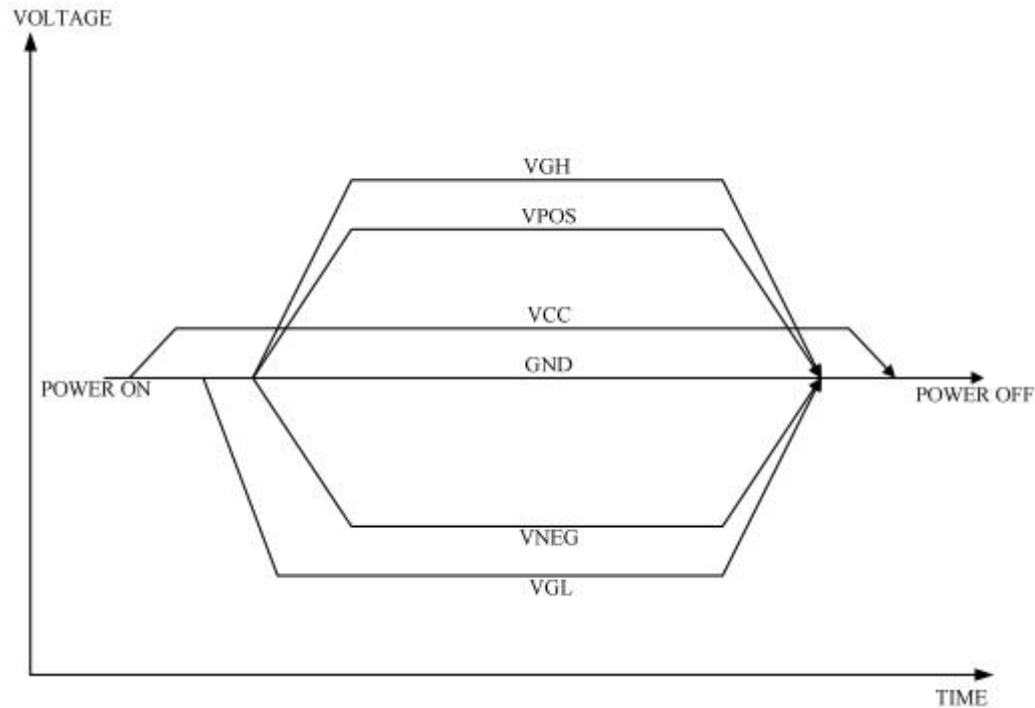
6. Electrical Specification

6.1 Power On/Off Sequence

This IC is a high-voltage EPD source driver, so it may be damaged by a large current flow if an incorrect power sequence is used.

Connecting the drive powers, [VNEG, VGL] and [VPOS, VGH] after the logical power, VCC, is the recommended sequence.

When shutting off the power, shut off the drive power and then the logic system or turn off all powers simultaneously.



Note: The minimum time is 12 μ s between "OE goes LOW" and "VPOS and VNEG power OFF"

6.2 AC Characteristics

6.2.1 Source AC Characteristic

For Source: (VCC=AVCC=3V, VPOS=15V, GND=0V, VNEG=-15V, VGL=-20V, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock CLK cycle time	t _{cy}	-	16.6	50	-	ns
D15...D0 setup time	t _{su}	-	8	-	-	ns
D15...D0 hold time	t _h	-	8	-	-	ns
STL1/STL2 setup time	t _{stls}	-	0.5 x t _{cy}	-	0.8 x t _{cy}	ns
STL1/STL2 hold time	t _{stlh}	-	0.5 x t _{cy}	-		ns
LE on delay time	t _{LEDLY}		3.5 x t _{cy}			
LE high-level pulse width	t _{LE}	-	300	-	-	ns
LE off delay time	t _{LEoff}	-	200	-	-	ns
Output settling time to +/- 30mV	t _{OUT}	Cload = 200pF		-	20	ns
LE off STL falling time	t _{is}	-	800	-		ns

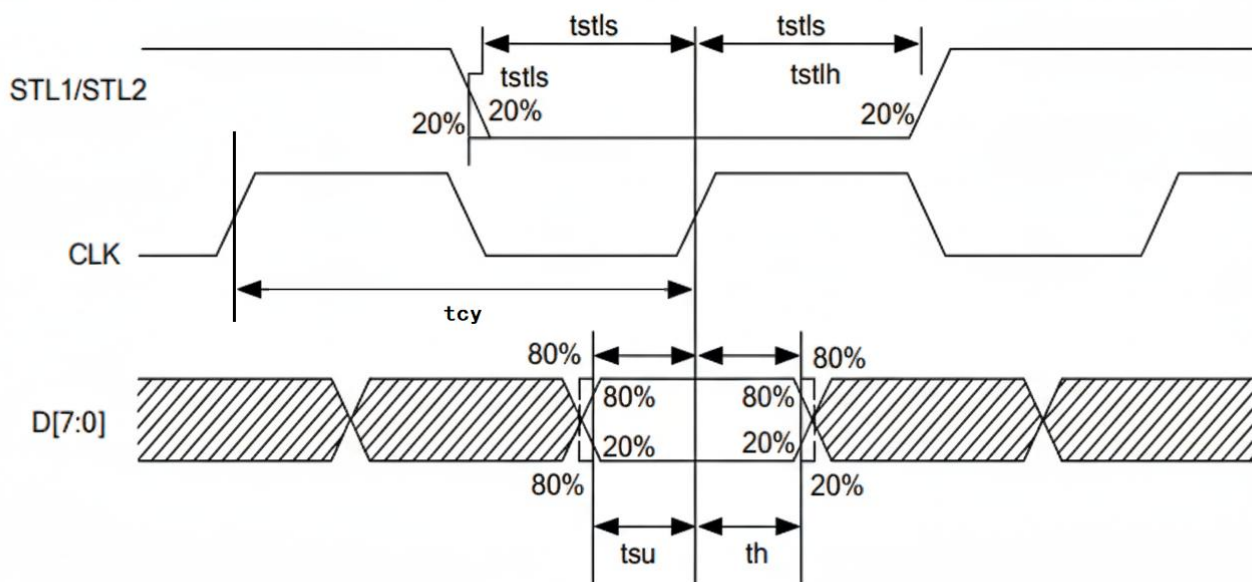
6.2.2 Gate AC Characteristic

For Gate: (VCC=1.8V-3.6V, VGH=22V, GND=0V, VGL=-20V, Ta=25°C)

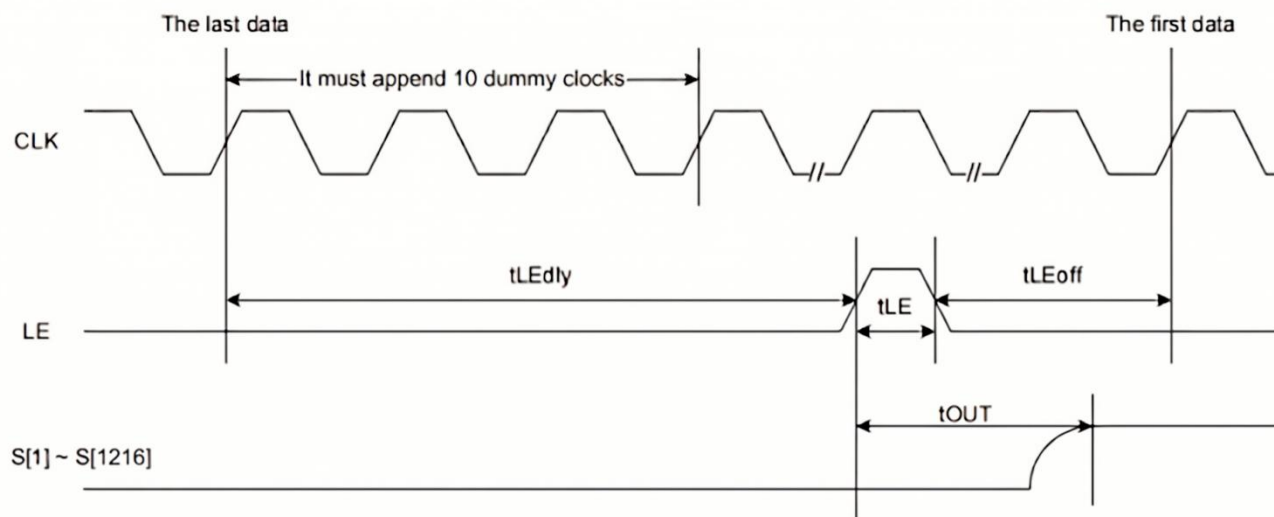
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock rise time	Trck	10% to 90%	-	-	100	ns
Clock fall time	Tfck	90% to 10%-	-	-	100	ns
Clock pulse width (low)	Tdkl		1000	-	-	ns
Clock pulse width (high)	Tckh	-	1000	-	-	ns
Clock frequency	Fclk	-	-	-	200	KHz
XON pulse width	TwXON	-	10	-	-	μs
XON to output delay time	Tpd	CL=300pF	-	-	20	μs
STV rise time	Trstv	10% to 90%	-	-	100	ns
STV fall time	Tfstv	90% to 10%	-	-	100	ns
STV setup to Clock	Tsu	-	100	-	Tclkh-100	ns
STV hold from Clock	Th	-	100	-	Tclkh-100	ns
Output transfer delay time	Td	CL=300pF	-	1000	-	ns
Output rise time	Tr	CL=300pF, 10% to 90%	-	-	1	us
Output fall time	Tf	CL=300pF, 90% to 10%	-	-	1	us
VCC rise time	Ton	-	-	-	20	ms
VCC fall time	Toff	-	-	-	20	ms
VCC waiting time	Toff-on	-	700	-		ms

6.3 Operating Timing

6.3.1 Source

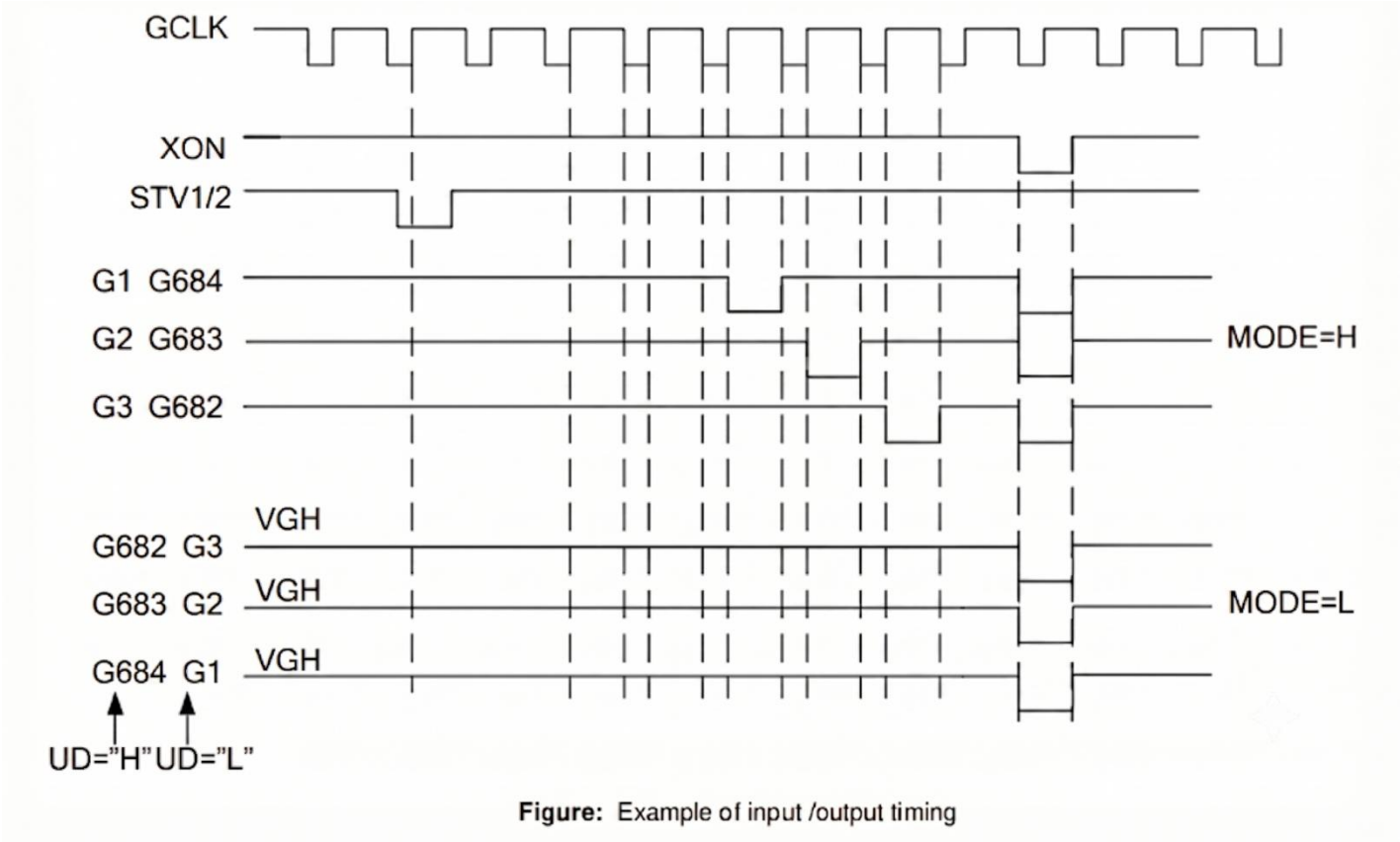


Clock and Data Timing



Output Latch / Control Signals

6.3.2 Gate



6.4 Timing Waveform

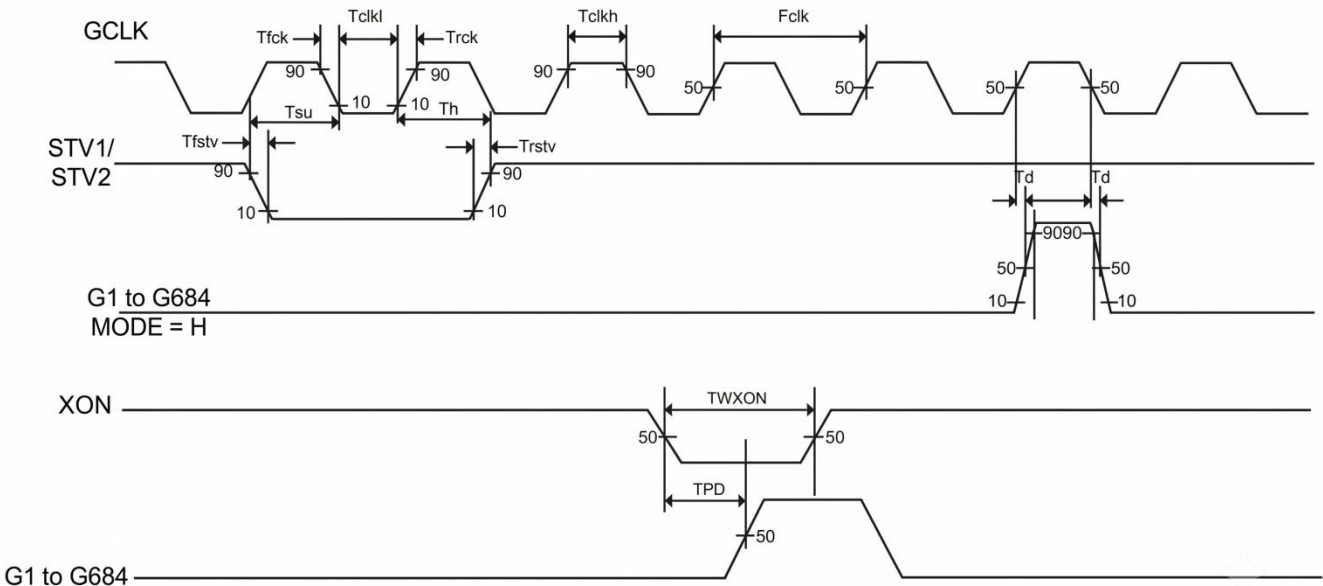


Figure: Timeing Waveform

6.5 VCC on/off time

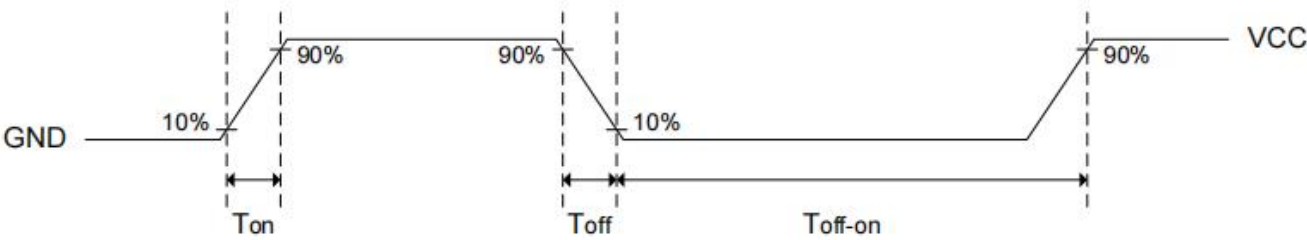


Figure 8. VCC on/off time

7.Mechanical Specifications

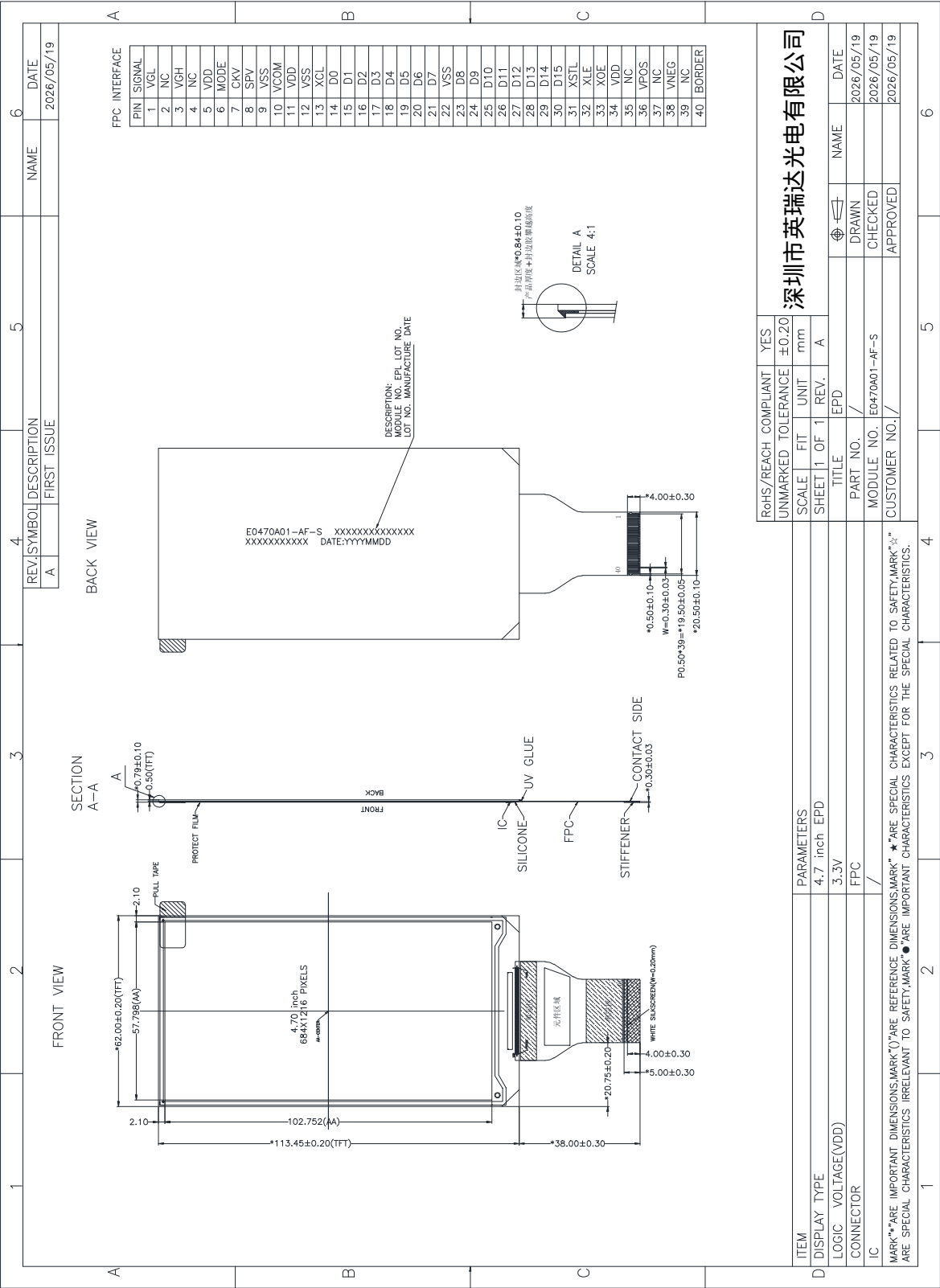
7.1 Dimension

Parameter	Specifications	Unit	Remark
Screen Size	4.70	Inch	
Display Resolution	684(H)×1216(V)	Pixel	DPI:297
Active Area	57.798×102.752	mm	
Pixel Pitch	0.0845×0.0845	mm	
Pixel Configuration	Rectangle		
Outline Dimension	62.00(H)×113.45 (V) ×0.79(D)	mm	

7.2 Electrical Connector

CONNECTOR	NUMBER OF PINS	MATING CONNECTOR
EPD Panel Connector	40	FPC pitch=0.5mm

7.3 Mechanical Drawing of EPD Module



8.Optical Characteristics

Parameter	Conditions	Values			Units	Notes
		Min	Typ	Max		
White Reflectivity	---	---	35.32	---	%	
Contrast Ratio (CR)	---	---	14:1	---		

Note:T_{amb}=25℃, f_v=85Hz. Measurements are made with Eye-One Pro Spectrophotometer

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

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10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T = +60°C, RH=40% ,240h Test in white pattern
3	High-Temperature Operation	T = +50°C, RH = 30% ,240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=+40°C, RH=90%,240h
6	High Temperature, High Humidity Storage	T=+60°C, RH=80%,240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)
9	UV exposure Resistance	765 W/m ² for 168hrs, 40°C ,Test in white pattern